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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,033	07/03/2003	Tadashi Iguchi	03180.0326	5852

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
11/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,033	IGUCHI ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,5,7-11 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,7-11,14,16,18,19 and 21* is/are allowed.

6)☒ Claim(s) *5,15 and 22* is/are rejected.

7)☒ Claim(s) *17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____. is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 5, 15, and 22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claims 17 and 20 are objected to because of the following informalities: the phrase "making a side wall spacer on a surface of each of said isolating fillers in a side wall of said floating gate electrodes" in claim 17 is incorrect since the spacer is not in the sidewall of the floating gate. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 5, 15, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hagiwara (JP 2001-274367).

5. In reference to claim 5, Hagiwara (JP 2001-274367) discloses a structure which meets the claim. Figure 29 of Hagiwara discloses a semiconductor memory comprising a memory cell array constituted by memory cells with each memory cell having a

floating electrode (140). The memory cells are arranged in a matrix on a semiconductor substrate (100). A plurality of first trenches is formed in the semiconductor substrate (100). Each first trench is formed between adjacent ones of said memory cells along a gate width direction. A plurality of isolating fillers (110) is filled in the first trenches. A plurality of second trenches is formed in the isolating fillers (110). Each second trench is formed between the floating electrodes (140) of adjacent ones of the memory cells along the gate width direction. The second trenches are in the shape of a U. A word line (160) is connected to the memory cells and is buried in the second trenches and extending along the gate width direction.

6. With regard to claim 22, the applicant has characterized a second trench which is capable of reducing parasitic capacitance as being shallower than the first trench and preferably reaches at least the surface of the well region (currently filed specification, p. 9, lines 16-21). The second trench of Hagiwara meets these characteristics thus meeting the claim. Furthermore, the applicant has characterized a second trench as reducing parasitic capacitance since the parasitic capacitance generated by the floating gate, the dielectric in the trench, and an insulating film of the trench, and at the word line is electrically connected in parallel to the parasitic capacitance between floating gates of the memory cells (currently filed specification, p. 3, lines 6-16). The second trench of Hagiwara also meets these characteristics as well and thereby meets the claim.

7. With regard to claim 15, Hagiwara (JP 2001-274367) discloses a method which meets the claim. Figure 29 of Hagiwara discloses a method of manufacturing a semiconductor memory which comprises making element isolating regions (110) by

forming a plurality of first trenches in a semiconductor substrate (100). Each first trench is made between adjacent ones of a plurality of memory cell forming regions along a gate width direction. The plurality of first trenches is filled with a plurality of isolating fillers. A plurality of floating gate electrodes (140) is formed on the semiconductor substrate (100) at the memory cell forming regions. The floating gate electrodes (140) have a predetermined gate width. A plurality of second trenches is formed in the isolating fillers filled in the first trenches. Each second trench is made between adjacent ones of the floating electrodes (140) along the gate width direction. The second trenches are made in the shape of a U. A word line (160) is formed in the second trenches. The word line (160) extends along the gate width direction.

Allowable Subject Matter

8. Claims 4, 7-11, 14, 16, 18, 19 and 21 are allowed.

9. The following is an examiner's statement of reasons for allowance: the examiner is unaware of any prior art which suggests or renders obvious a semiconductor memory or its method of fabrication with a wordline embedded within a trench that is itself formed within a trench insulation structure such that the wordline trench has an inverted trapezoidal shape as suggested in claims 4 and 14.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KVQ

/ A. Sefer /
Primary Examiner
AU 2826